

## Chapter 4 Resistor-Transistor Logic

Resistor-transistor logic, RTL, is an old technology that is no longer commercially available. It is a useful starting place to study logic gates because it is a logical extension of the transistor inverter studied in the previous chapter, and because it is a useful circuit in itself.

A two-input gate is shown in Figure 1. As with most logic, the transistors operate only in saturation or cutoff. There are four possible combinations of logic inputs, L-L, L-H, H-L, and H-H for inputs A and B respectively. A low input will cutoff the associated transistor, and a high input will saturate it. Figure 2 shows these combinations where the transistors have been replaced by their corresponding models. If both transistors are cutoff, the output will be high, 3.0 Volts. If either transistor is saturated, the output will be 0.2 Volts, or low. The truth table for this gate is given in Figure 3 and shows that the gate performs a logic NOR function.

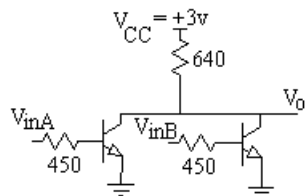
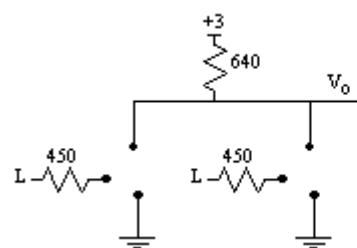


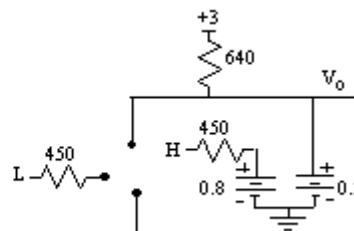
Figure 1. RTL gate

$V_{inA}$	$V_{inB}$	$V_o$
L	L	H
L	H	L
H	L	L
H	H	L

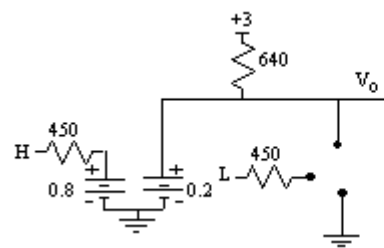
Figure 3. Truth table for RTL gate



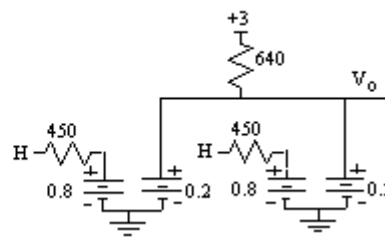
a. L-L inputs



b. L-H inputs



c. H-L inputs



d. H-H inputs

Figure 2. RTL gate with four combinations of inputs

Our job is to determine the eight terminal specifications, input and output voltages and currents when these terminals are both high and low as shown in Table 1. Definitions of these terms are given in Appendix A.

Table 1. The Eight Terminal Specifications to be Determined.

$V_{inH}$	$V_{inL}$	$I_{inH}$	$I_{inL}$
$V_{oH}$	$V_{oL}$	$I_{oH}$	$I_{oL}$

We begin the calculation of the terminal specification by noting that when a transistor is saturated, the collector-emitter voltage is 0.2 volts. The output terminal is connected directly to the collector terminal, thus,  $V_{oL} = 0.2$  volts. Assume the gate on which this analysis is taking place is embedded in a logic system. Its inputs are driven by other identical logic gates. Then if the outputs of those driver gates are logic low, the inputs to the device under analysis are low. We will use this as a starting place for the calculations.

$$V_{inL} = 0.2, \text{ (LOW input to both transistors)}$$

Under this condition, both transistors will be cutoff, making the output high. The circuit diagram with circuit models for the cutoff transistors is shown in Figure 4. The output voltage then is 3.0 Volts. We will call this a no-load condition when there is no load connected to the output.

$$V_{oH} = 3.0 \text{ Volts (No-Load)}$$

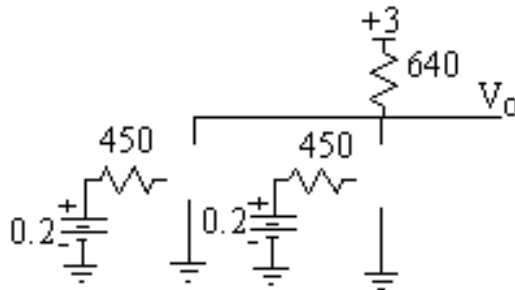


Figure 4. RTL gate with both inputs low. The transistors are replaced by the cutoff model.

Also note from Figure 4 that the input current is zero because the transistor is cutoff. Thus,

$$I_{inL} = 0$$

The question naturally arises about how high the input voltage may rise and still keep the transistor cut off. The input voltage must stay below  $V_{BE\gamma}$  to guarantee the transistor is off, making

$$V_{inLmax} = 0.5 \text{ Volts.}$$

The maximum value is given in this case because we need to know how high it may rise. This means that the input voltage may rise as high as 0.5 volts and still keep the transistors off, and will always be recognized by the gate as a "low".

## INPUT HIGH

In this case we want the transistor to be saturated. Either transistor saturated will cause the output to go low, to 0.2 volts. This case is shown in Figure 5. We show the circuit with one of the transistors cutoff, although both saturated would produce the same result. We start by determining the minimum input current that will keep the transistor in saturation.

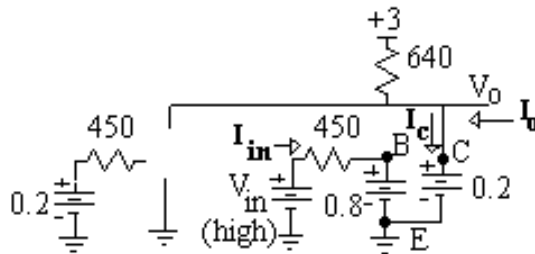


Figure 5. RTL gate with one input high.

$$I_{Csat} = \frac{3.0 - 0.2}{0.640k} = 4.375mA$$

The minimum base current to keep the transistor saturated is (assuming  $\beta=30$ )

$$I_{inHmin} = \frac{I_{Csat}}{\beta} = \frac{4.375}{30} = 0.146mA$$

The minimum value is of interest because this current is dependent on the input voltage. From this value, we can determine the minimum input voltage that will be guaranteed to be recognized as a "high".

$$V_{inHmin} = 0.8 + 0.146 \text{ mA} \times 0.450 \text{ K}\Omega = 0.866 \text{ Volts}$$

Any input voltage greater than or equal to 0.866 volts will cause the transistor to be saturated, and thus be recognized as a "high". We previously found  $V_{inLmax} = 0.5$  volts. Any input voltage between 0.5 and 0.866 is an invalid logic level and the manufacturer assumes no responsibility if you provide an input voltage in that range. For the gate with no load, the relationships between input and output voltages are presented graphically in Figure 6. The noise margins NMH and NML are defined in Appendix A.

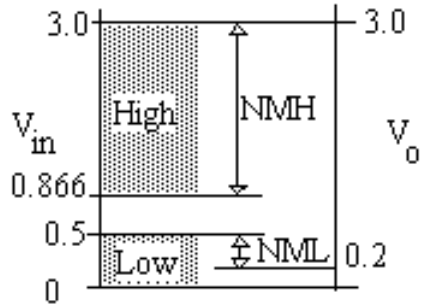


Figure 6. Graphical representation of input voltage ranges and output voltages for the unloaded RTL gate.

### CALCULATIONS WHEN THE GATE IS USED TO DRIVE OTHER GATES

Up to this point we have done all calculations assuming no load on the gate. While convenient for visualization, it is not a very useful situation. Let us look at the loading of the gate as if it were embedded in a logic system driving identical gates as shown in Fig. 7.

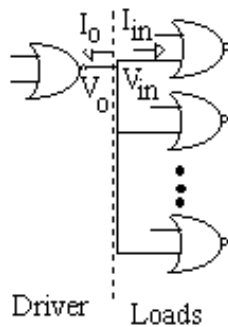


Figure 7. Driver gate being analyzed driving load gates.

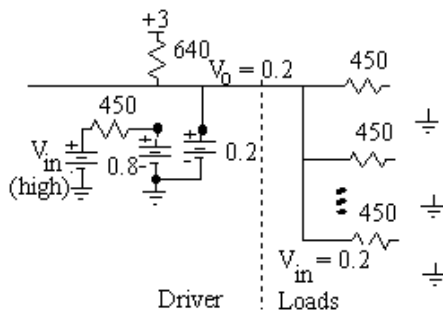


Figure 8. Driver with loads when driver output is low.

There are two cases, the driver output being low as shown in Figure 8, and the driver output being high as shown in Figure 9. When the output is high, the driver transistor is saturated and the output is 0.2 Volts. All the input transistors of the load gates are cutoff and no current flows. The output voltage remains at 0.2 volts, unchanged by the loads.

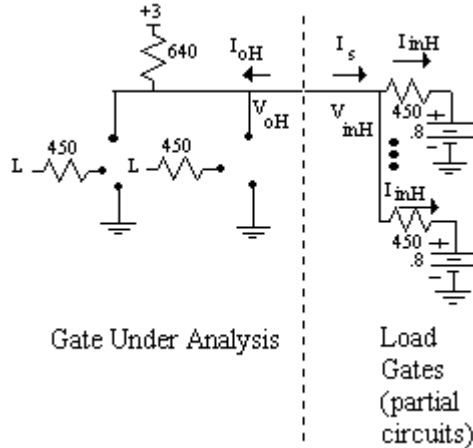


Figure 9. RTL gate with N loads when driver output is high.

However, when the output is high, the load gates require current, pulling the output voltage down. This situation is shown in Figure 9 with an unspecified number of loads. How many can you connect and still expect the gates to work right? This is called the maximum fanout. The output voltage is determined by the load current being SOURCED by the driver.

$$V_{oH} = 3.0 - I_s \times 0.64 \text{ k}\Omega$$

Where the current coming out of the driver gate is divided between the load gate inputs. Since the minimum voltage at the load gate inputs when high is 0.866 Volts, this is the lowest the output voltage of the driver gate may go. Thus,

$$I_{oH \max} = -\frac{3.0 - 0.866}{0.64k} = -3.334 \text{ mA}$$

The negative sign comes about because currents are always defined as positive when going into the terminal. Each load requires a minimum of 0.146 mA as input current, therefore, the maximum fanout is

$$\text{MaxFanout} \leq \frac{3.334}{0.146} = 22.8$$

Thus, the maximum fanout is 22.

## PRACTICAL FANOUT

The maximum fanout will not provide for any noise margin. Also, manufacturing tolerances will not allow such close calculations. Therefore, most manufacturers limit the allowed fanout to a much smaller number than found by nominal and typical calculations. Typically, the fanout would be limited to say 5 loads. In this case, the output voltage under maximum load would be substantially higher than calculated above. With five loads, the output current will be

$$I_{oH} = -\frac{3.0 - 0.8}{0.64 + \frac{0.45}{5}} = -3.014mA$$

and the output voltage will be

$$V_{oH} = 3.0 - I_{oH} \times R_C = 3.0 - 3.014 \text{ mA} \times .64 \text{ k}\Omega = 1.071 \text{ Volts}$$

Under this condition, the Noise Margin High is

$$NMH = 1.071 - 0.866 = 0.205 \text{ Volts}$$

Note that in many cases the output voltage will be higher than the value just calculated and thus the noise margin larger. If we define the maximum allowed fanout to be five, then  $V_{oHmin} = 1.071 \text{ Volts}$ .

#### CALCULATION OF $I_{oL}$

If we define the maximum allowed fanout to be five, then the minimum voltage ever seen by the input will be 1.071 Volts. The minimum current into the input will be

$$I_{inHmin} = \frac{1.071 - 0.8}{0.45k} = 0.602mA$$

The maximum collector current is  $\beta$  times this or 18.067 mA and still stay in saturation. Thus, the maximum output current when the output is low is this current minus the current down through the 640  $\Omega$  resistor.

$$I_{oLmax} = 18.067 - 4.375 = 13.692 \text{ mA}$$

We now have all the specifications for this gate. The results are shown in Table 2. We have assumed here that the fanout is limited to 5 loads. There is a certain amount of arbitrariness in the choice of  $V_{oH}$  and  $I_{oH}$ . Many other performance requirements could have been chosen. The values given are self consistent, however. First note that  $V_{oHmin} > V_{inHmin}$  and  $V_{oLmax} < V_{inLmax}$ , as shown in Figure 10. The voltages are compatible.

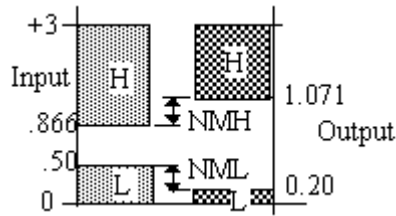


Figure 10. Voltage compatibility chart, with 5 loads

To determine fanout,

$$\frac{I_{oH}}{I_{inH}} = 5.007 \quad \text{and} \quad \frac{I_{oL}}{I_{inL}} = \infty$$

Therefore, the fanout is 5.

Table 2. Terminal specifications for the RTL Gate

$V_{inLmax} = 0.500$ Volts	$V_{oL} = 0.2$ Volts
$V_{inHmin} = 0.866$ Volts	$V_{oHmin} = 1.071$ Volts (N=5)
$I_{inL} = 0$	$I_{oLmax} = 13.692$ mA ( $V_{in} > V_{oHmin}$ )
$I_{inHmin} = 0.602$ mA	$I_{oHmax} = -3.014$ mA

### INTERFACING TO RTL

Table 2 is a set of specifications that would be provided by the manufacturer of the RTL logic. From this information, you would be expected to be able to use the gates without exceeding any specification. Any gate embedded in a logic system using only the RTL gates analyzed, would be guaranteed to work within the specifications. The only limitation we must follow is limiting the fanout to five loads. However, logic is rarely used without interfacing to the outside world at some point. There must be some signals at some point that are generated outside the logic system that must be recognized as a logic one or a zero. Similarly, there is usually some point where a logic gate output must drive a device that is not another gate.

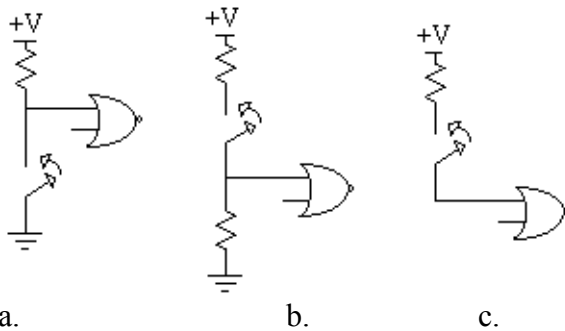


Figure 11. Three possible configurations of a switch-to-logic gate interface.

Figure 11 shows three possible connection using a switch to generate the logic inputs to a gate. In Figure 11a the switch is used as a pull-down to make the input voltage a logic zero when the switch is closed. The resistor pulls the input voltage up to a logic one when the switch is open. Looking at the specifications in Table 2, we note that when the switch is closed, the input voltage is zero volts, well below the required  $V_{inLmax}$  of 0.5 volts. The gate input current is zero so the switch needs only to handle the current coming down through the resistor. When the switch is open, current will come down through the resistor into the gate input terminal. The specifications show the voltage must be above 0.866 volts and the current must be at least 0.602 mA. From these values, we can select a value of  $R_1$ . To provide a noise margin, we should certainly provide a voltage at least as high as  $V_{OHmin} = 1.071$  volts. Let's shoot for 2.0 volts to provide even greater noise margin. We know this will provide greater than the minimum current, but we don't yet know how much. We now have to put on our engineer's hat and look inside the gate to finish the design. The parts of the circuit that pertain to this case are shown in Figure 12 with only the base-emitter voltage of the transistor shown. The transistor must be in saturation so we use 0.8 volts for  $V_{BEsat}$ .

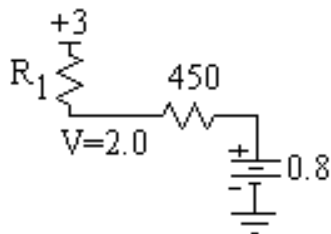


Figure 12. Circuit with switch open.

Solving this circuit, we can write a single node equation at the input node,  $V_{in} = 2.0$  v,

$$(3.0-2.0)/R_1 = (2.0-0.8)/450$$

Solving, we get  $R_1 = 375 \Omega$ . This is not a standard resistor value so we would select a nearby standard value and re-solve the circuit, this time to determine the input voltage. If we are satisfied with the result, then we are finished. If the input voltage found is not satisfactory, we would try with another value. Note that we do not have to get 2.0 volts, we simply chose that value as a place to start the design. We do, however, have to provide  $V_{in} > V_{inHmin}$ .

The design of the circuit in Figure 11b would follow a similar track. Notice that in this circuit the input voltage is high when the switch is closed; the opposite of the circuit in Figure 11a. Figure 11c is simpler than 11b, but it is not recommended because when the switch is open, the input lead of the gate is floating or disconnected and susceptible to noise which might cause random errors in the logic.

Figure 13 shows an example of an interface at the output of the gate. In this case, we want to drive an LED at 30 mA. Neither the high nor low output currents of the gate are sufficient, so we use a transistor as a current amplifier. Many other configurations are possible and some may be preferable depending on the application. We will not go through the design of this circuit here. A similar circuit was designed at the end of the previous chapter.

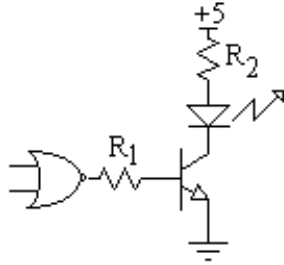


Figure 13. Example of an output interface circuit.

## EXERCISE

Mountain State Electronics, Inc. has provided a data sheet for its line of RTL NOR gates:

$$V_{inLmax} = 0.45 \text{ volts}$$

$$V_{oLmax} = 0.3 \text{ volts}$$

$$V_{inHmin} = 0.85 \text{ volts}$$

$$V_{oHmin} = 1.00 \text{ volts (@N=5)}$$

$$I_{inL} = 0.0 \text{ mA}$$

$$I_{oLmax} = 10.00 \text{ mA (@ } V_{in} > V_{oHmin} \text{)}$$

$$I_{inHmin} = 1.00 \text{ mA}$$

$$I_{oHmax} = -5.50 \text{ mA (@ } V_o = V_{oHmin} \text{)}$$

1. Determine:

$$\text{Fanout} = \underline{\hspace{2cm}}$$

$$\text{NMH} = \underline{\hspace{2cm}}$$

$$\text{NML} = \underline{\hspace{2cm}}$$

2. For the logic network below, write the logic level ( H or L ) at each node.

3. If you used a voltmeter to measure the voltage, what voltage would you expect to measure at each node? (Use <, > signs to describe the voltages. These voltages will be the thresholds you will use to determine if the network is operating properly.)

$$V_A \underline{\hspace{1cm}} \quad V_C \underline{\hspace{1cm}} \quad V_E \underline{\hspace{1cm}} \quad V_G \underline{\hspace{1cm}}$$

$$V_B \underline{\hspace{1cm}} \quad V_D \underline{\hspace{1cm}} \quad V_F \underline{\hspace{1cm}} \quad V_H \underline{\hspace{1cm}}$$

4. Beside each connecting wire, draw an arrow showing the direction of the actual current in the wire. Write  $I = 0$  if no current flows.

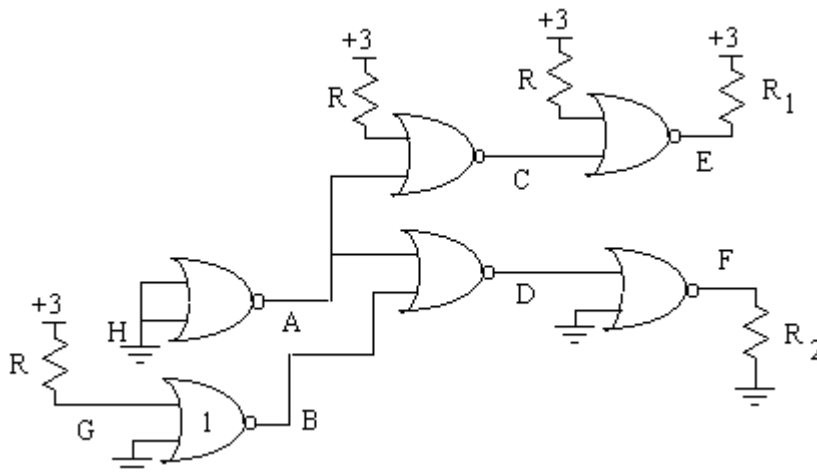
5. In each wire labeled A-H, estimate the magnitude of the current.

$$I_A \underline{\hspace{1cm}} \quad I_C \underline{\hspace{1cm}} \quad I_E \underline{\hspace{1cm}} \quad I_G \underline{\hspace{1cm}}$$

$$I_B \underline{\hspace{1cm}} \quad I_D \underline{\hspace{1cm}} \quad I_F \underline{\hspace{1cm}} \quad I_H \underline{\hspace{1cm}}$$

6. Determine the maximum allowable value of the pull-up resistor R at the input of gate #1.

$$R_{max} = \underline{\hspace{2cm}}$$



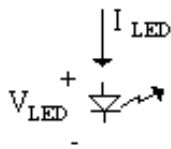
**In-Class Design Exercise:**

Assume RTL Specifications are given by manufacturer:

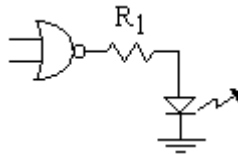
**Terminal Specifications:**

- $V_{inLmax} = 0.5$  volts       $I_{inL} = 0$
- $V_{inHmin} = 0.866$  volts       $I_{inHmin} = 0.602$  mA For max  $I_{oL}$
- $V_{oL} = 0.2$        $I_{oLmax} = 13.692$  mA @  $V_{inH} > V_{oHmin}$
- $V_{oH} = 1.071$  @ Fanout = 5       $I_{oHmax} = -3.014$  mA

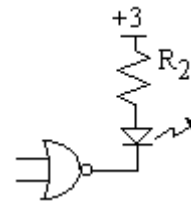
1. Drive an LED from an RTL gate.



LED Model:  
 $V_{LED} = 1.8$  for  $I > 0$   
 $I = 0$  for  $V_{LED} < 1.8$



Method 1



Method 2

Performance Requirement:  
 $9 \text{ mA} < I_{LEDon}$

Constraints:  
 Use 5% standard value resistors, nominal calculations  
 3-volt power supply

Method 1      How does it work? (Draw the currents on the diagram)

When gate output is low LED is \_\_\_\_\_

When gate output is high LED is \_\_\_\_\_

How much current is available to turn on the LED? \_\_\_\_\_

$R_1 =$  \_\_\_\_\_

Method 2 How does it work? (Draw the currents on the diagram)

When gate output is low LED is \_\_\_\_\_

When gate output is high LED is \_\_\_\_\_

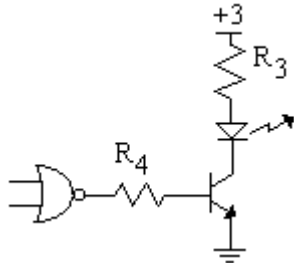
How much current is available to turn on the LED? \_\_\_\_\_

\_\_\_\_\_ <  $R_2$  < \_\_\_\_\_

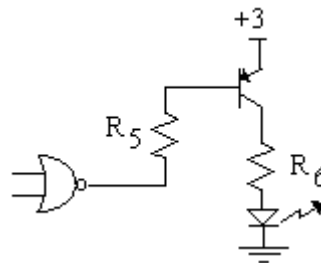
2. Same problem, except the performance requirement:

$$20 \text{ mA} < I_{LED} < 25 \text{ mA}$$

Suggested Methods:



Method 3



Method 4

Assume the following transistor specifications:  
 $V_{BE\gamma} = 0.5$ ,  $V_{BEsat} = 0.8$ ,  $V_{CEsat} = 0.2$ ,  $\beta = 10$   
 (negative voltages for pnp)

Method 3 How does it work? (Draw the currents on the diagram)

When gate output is low, the transistor is \_\_\_\_\_, and LED is \_\_\_\_\_

When gate output is high, the transistor is \_\_\_\_\_, and LED is \_\_\_\_\_

How much current is available to saturate the transistor \_\_\_\_\_  
 to turn on the LED? \_\_\_\_\_

$R_{3min} =$  \_\_\_\_\_, \_\_\_\_\_ <  $R_4$  < \_\_\_\_\_

Designer's choice:  $R_4 =$  \_\_\_\_\_, then  $I_{Csat} =$  \_\_\_\_\_,  $I_{Bmin} =$  \_\_\_\_\_

$R_{3max} =$  \_\_\_\_\_

Method 4 How does it work? (Draw the currents on the diagram)

When gate output is low, transistor is \_\_\_\_\_, and LED is \_\_\_\_\_

When gate output is high, transistor is \_\_\_\_\_, and LED is \_\_\_\_\_

How much base current is available to saturate the transistor \_\_\_\_\_

What is the maximum collector current is available to turn on the LED? \_\_\_\_\_

$R_{5min} = \underline{\hspace{2cm}}$ ,  $\underline{\hspace{2cm}} < R_6 < \underline{\hspace{2cm}}$

Designer's choice:  $R_6 = \underline{\hspace{2cm}}$ , then  $I_{Csat} = \underline{\hspace{2cm}}$ ,  $I_{Bmin} = \underline{\hspace{2cm}}$

$R_{5max} = \underline{\hspace{2cm}}$

### Problems

Mountaineer Logic Inc. is developing a new line of RTL logic NOR gates. The gates are said to have a fanout of 5 and the following component values:

$$V_{CC} = 5.0 \text{ Volts}, R_C = 470 \text{ Ohms}, R_B = 1.5 \text{ K Ohms}, \text{ and } \beta_{min} = 20.$$

1. For the RTL gate above, present the following specifications in tabular form:

Noise margins NMH and NML,  $V_{OL}$ ,  $V_{OH}$  (at  $N=5$ ),  $V_{inLmax}$ , and  $V_{inHmin}$ .

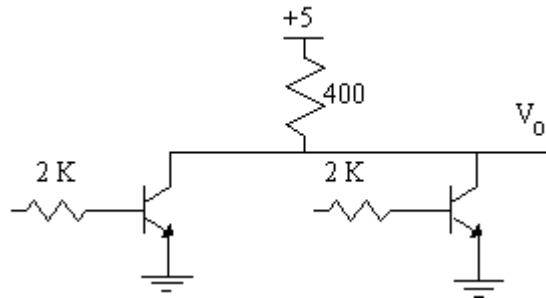
2. Draw the voltage transfer characteristic ( $V_o$  vs  $V_{in}$ ) for the gate.

3. Determine the absolute maximum fanout with zero noise margin.

4. The RTL gate shown below has a specified "high" noise margin, NMH, of 1.00 volts. What is the specified fanout?

The transistors model parameters are:

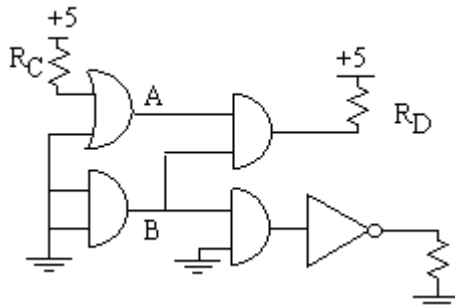
$V_{BEcutin} = 0.5$  volts,  $V_{BEsat} = 0.8$  volts,  $V_{CEsat} = 0.2$  volts,  $\text{Beta} = 12$



5. A logic family has the following terminal specifications:

$V_{inLmax} = 0.6$	$V_{oLmax} = 0.4$
$V_{inHmin} = 1.8$	$V_{oHmin} = 2.4$
$I_{inL} = -1.0$ mA	$I_{oLMax} = 10$ mA
$I_{inH} = 1.0$ mA	$I_{oHmax} = -5$ mA

This family of logic gates is used in the following logic system.



What voltage do you expect at nodes A and B?

What values of resistors  $R_C$  and  $R_D$  can be used? (Specify max or min.)